(54) Title: IMAGE PROCESSOR AND IMAGE DISPLAY APPARATUS PROVIDED WITH SUCH IMAGE PROCESSOR
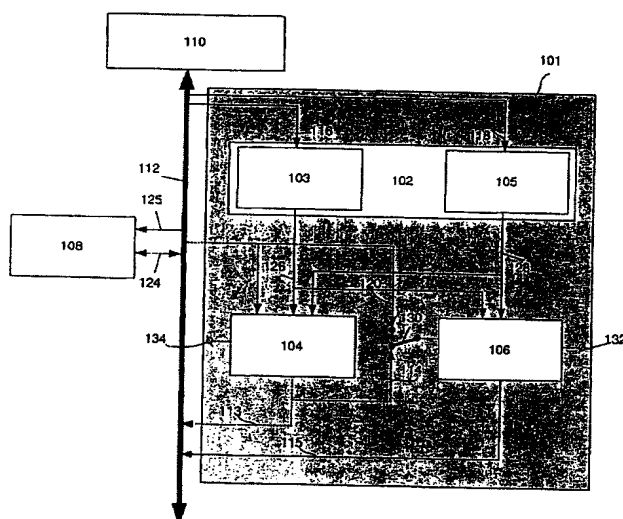
(57) Abstract: The image processor (101) for motion compensated image processing comprises a motion compensation unit (106) for calculating an output image based on a particular motion vector field and based on a first input image and a second input image. The particular motion vector field can be calculated by a motion estimator (104) which is part of the image processor (101) or by an external unit (108). The image processor (101) is designed to select from which source, i.e. the motion estimator (104) or the external unit (108), the particular motion vector field is taken to calculate the output image. The external source is designed to calculate the particular motion vector field based on a motion vector field which was provided by the motion estimator (104) of the image processor (101).

Image processor and image display apparatus provided with such image processor

The invention relates to an image processor for motion compensated image processing, comprising:

- a memory unit for storing a first input image and a second input image;

- a motion estimator for estimating a motion vector field based on the first

5   input image and the second input image; and

- a motion compensation unit for calculating an output image based on a further motion vector field and based on the first input image and the second input image.

The invention further relates to an image display apparatus comprising:

- a receiver for receiving a sequence of images comprising a first input image

10   and a second output image;

- an image processor for motion compensated image processing, comprising:

- a memory unit for storing the first input image and the second input image;

- a motion estimator for estimating a motion vector field based on the first

input image and the second input image; and

15   - a motion compensation unit for calculating an output image based on a further motion vector field and based on the first input image and the second input image;

- a display device for displaying the output image.

20   An embodiment of the image processor of the kind described in the opening paragraph is known from the article "IC for motion-compensated de-interlacing, noise reduction, and picture rate conversion", by G. de Haan, in IEEE Transactions on Consumer Electronics, Vol. 45, No. 3, August 1999.

Image sequences come in various image rates: film material in 24, 25 and 30

25   Hz and video usually in 50 Hz and 60 Hz. Television displays, on the other hand, are commercially available with image rates of 50, 60 and 100 Hz, and have either progressive or interlaced scanning. Simple image rate converters repeat images until the next image arrives, which results in blur and/or judder when motion occurs. Similarly, de-interlacing sometimes results from repetition, or averaging of neighboring lines. The more advanced de-interlacing

concepts apply vertical-temporal processing, but even these degrade those portions of images where motion occurs.

In the cited article it is described that consumer television ICs appeared in the mid-nineties using motion estimation and motion compensation to achieve high performance conversion for even moving sequences. The article shows improved algorithms for motion estimation, motion compensated de-interlacing, motion compensated image interpolation and motion compensated noise reduction. The IC implementing these algorithms comprises a memory unit to cache a current and a previous image, a motion estimator and a motion compensation unit. The working of the IC is as follows. Two consecutive input images are received and cached in the memory unit of the IC. Based on these input images motion vectors are calculated. The set of motion vectors of one image pair, i.e. a current and a previous image, is called a motion vector field. The motion vectors are provided to the motion compensation unit which performs the operations as listed above. The result is a motion compensated output image. The IC performs the operations in real-time. This means that a motion estimation algorithm with a relatively low operation count is implemented. Although the results of the motion estimation unit are relatively good, there can be erroneous motion vectors, resulting in artifacts in the motion compensated images. Especially at the borders of the images or at occlusion areas in the images. More advanced motion estimation is required in these cases.

It is a first object of the invention to provide an image processor of the kind described in the opening paragraph that is designed to enable more advanced motion estimation.

It is a second object of the invention to provide an image display apparatus of the kind described in the opening paragraph with more advanced motion estimation.

The first object of the invention is achieved in that the image processor is designed to selectively receive the further motion vector field from:
- the motion estimator; or from
- an external unit.

The main difference with the image processor of the prior art is that the motion vectors can be calculated by the motion estimator of the image processor itself but that the motion vectors can also be calculated by an external unit, i.e. a source not being part of the processor itself, which is arranged to act as co-processor. It is preferred that this co-

processor is designed to perform more advanced motion estimation than the motion estimation of the motion estimator. Notice that the further motion vector field may correspond to the motion vector field calculated by the motion estimator but that it also may be a motion vector field which has been provided by the external unit.

5   An embodiment of the image processor according to the invention is designed to provide the motion vector field to the external unit which is arranged to calculate the further motion vector field on the basis of the motion vector field. In this embodiment the motion vectors can be exchanged to the external unit which is arranged to act as co-processor to improve the motion vector field which is calculated by the motion estimator of the image

10   processor. The advantage is that the available motion estimator of the image processor is used and the resulted motion vector field is improved by the external unit. The image processor has two modes of operations:

- One pass mode: The first input image and the second input image are received and stored in the memory unit of the image processor. Motion vectors are calculated

15   based on these input images. These motion vectors are provided to the motion compensation unit which calculates the motion compensated output image.

- Two pass mode: In the first pass of the two passes, the first input image and the second input image are received and stored in the memory unit. Motion vectors are calculated based on these input images. These motion vectors are provided to the external

20   unit. Externally the received motion vector field can be temporarily stored. But most important, the external unit is arranged to perform operations on the motion vector field in order to improve it. In the mean time the image processor can continue with processing other images. E.g. the motion compensation unit of the image processor can calculate a second motion compensated output image or the motion estimator of the image processor can

25   calculate a motion vector field of another image pair. In the second pass of the two passes, the further motion vector field corresponding to the first and second input image are provided to the motion compensation unit together with the first and second input image. Based on this input the output image is calculated.

In the two pass mode the first and the second input image have to be read into

30   the memory unit twice: once for the first pass and once for the second pass. The result is an additional load of the memory bus. However the main advantage of the image processor according to the invention which is designed to alternate between the one pass and the two pass mode is the scalability. It allows to choose between an increased image quality at the cost of some additional bandwidth.

In another embodiment of the image processor according to the invention, in which the motion vector field is provided to the external unit, the external unit is arranged to recalculate a particular motion vector of the motion vector field. Even more advanced adaptations of the motion vector field can be applied. E.g. by using extended sets of candidate motion vectors to find an appropriate motion vector. Motion estimation based on more than two consecutive images also belongs to the possibilities.

An embodiment of the image processor according to the invention, in which the motion vector field is provided to the external unit, comprises a switch with:

- a first input connector that is coupled to the motion estimator;
- a second input connector that is coupled to the external unit; and
- an output connector that is coupled to the motion compensation unit,

the switch having:

- a first state in which the first input connector is connected to the output connector; and
- a second state in which the second input connector is connected to the output connector.

The advantage of the switch is that it makes the design of the motion compensation unit relatively easy. The motion compensation unit comprises one interface to which with the appropriate motion vector fields are provided in stead of two interfaces which potentially can provide the further motion vector field.

In an embodiment of the image processor according to the invention, in which the motion vector field is provided to the external unit, the motion estimator comprises a first control interface in order to enable and/or disable the motion estimator. The advantage of the first control interface is that it makes the design of the motion estimator unit relatively easy. A main part of the timing and control of the motion estimator is executed externally to the motion estimator.

In an embodiment of the image processor according to the invention, in which the motion vector field is provided to the external unit, the motion compensation unit comprises a second control interface in order to enable and/or disable the motion compensation unit. The advantage of the second control interface is that it makes the design of the motion compensation unit relatively easy. A main part of the timing and control of the motion compensation unit is executed externally to the motion compensation unit.

In an embodiment of the image processor according to the invention the motion compensation unit is designed to perform at least one of the following operations:

- De-interlacing: Common video broadcast signals are interlaced, which implies that successive images contain only the even or only the odd lines alternately. De-interlacing attempts to restore the full vertical resolution, i.e. make both the odd and even lines available for each image;

- Temporal image interpolation: From a series of original input images a larger series of output images is calculated. Output images are temporally located between two original input images; and

- Temporal noise reduction. This can also involve spatial processing, resulting in spatial-temporal noise reduction.

The second object of the invention is achieved in that the image processor of the image display apparatus is designed to select a source from a set of sources, the source providing the further motion vector field to the motion compensation unit and the set of sources comprising:

- the motion estimator; and

- an external unit to which the motion vector field is provided.

Modifications of the image processor and variations thereof may correspond to modifications and variations thereof of the image display apparatus described.

These and other aspects of the image processor and of the image display apparatus according to the invention will become apparent from and will be elucidated with respect to the implementations and embodiments described hereinafter and with reference to the accompanying drawings, wherein:

Fig. 1A schematically shows an embodiment of the image processor in its context;

Fig. 1B schematically shows an embodiment of the image processor comprising a switch to select between motion vectors from the motion estimator or from the external unit;

Fig. 2 schematically shows the data flow of the motion vector field in an embodiment of the image processor running in the one pass mode;

Fig. 3A schematically shows the data flow of the motion vector field in an embodiment of the image processor during the first pass of the two pass mode;

Fig. 3B schematically shows the data flow of the further motion vector field in an embodiment of the image processor during the second pass of the two pass mode; and

Fig. 4 schematically shows an image display apparatus according to the invention.

Corresponding reference numerals have the same meaning in all of the Figures.

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Fig. 1A schematically shows an embodiment of the image processor 100 in its context. The image processor 100 comprises:

- a memory unit 102 for storing a first input image and a second input image;

- a motion estimator 104 for estimating a motion vector field based on the first

10 input image and the second input image; and

- a motion compensation unit 106 for calculating an output image based on a further motion vector field and based on the first input image and the second input image.

The image processor 100 is designed to select a source from a set of sources, the source providing the further motion vector field to the motion compensation unit 106 and

15 the set of sources comprising:

- the motion estimator 104; and

- an external unit 108.

The data bus 112 is designed to exchange e.g. data of input and output images and motion vectors. To the data bus 112 are connected:

20   - the image processor 100;

- an external memory device 110 arranged to store e.g. data of input and output images and motion vectors; and

- the external unit 108.

The working of the image processor is as follows. A first and a second input

25 image are retrieved from the external memory device 110 via the data bus 112 and stored in the memory unit 102. It is possible that all pixels of the first and second input image are stored in the memory unit 102 simultaneously. But preferably only a portion of these pixels is simultaneously stored in the memory unit 102. The first and the second input image are exchanged via image data path 116 and image data path 118, respectively. In the case that no

30 motion vector field of this image pair has been calculated before, the first and the second input image are provided to the motion estimator 104. The motion estimator 104 calculates the motion vector field and provides this to the motion compensation unit 106 via motion vector path 114. The first and the second input image are also provided via the image data paths 126 and 128 to the motion compensation unit 106, which calculates the corresponding

output image. In the case that a motion vector field of this image pair has been calculated before the further motion vector field is retrieved from the external source 108 and provided to the motion compensation unit 106 via motion vector path 120 together with the first and the second input image. Based on this input the motion compensation unit 106 calculates the

5   corresponding output image. The output image is exchanged via image data path 115. Image data is provided to the external unit 108 via image data path 125 and motion vectors are retrieved from the external unit 108 via motion vector path 123. The motion compensation unit 106 is designed to perform at least one of the following operations:

                    - de-interlacing;

10   - temporal image interpolation; or

                    - temporal noise reduction.

        Preferably the motion estimator 104 and of the motion compensation unit 106 operate according to algorithms as described in the article "IC for motion-compensated de-interlacing, noise reduction, and picture rate conversion", by G. de Haan, in IEEE

15   Transactions on Consumer Electronics, Vol. 45, No. 3, August 1999. Optionally the de-interlacing is performed in accordance with another method as described in "De-interlacing-An Overview" by G. de Haan, in proceedings of the IEEE, Vol. 86, No. 9, September 1998.

        It is preferred that the image processor is implemented on one IC. Alternatively, the image processor is implemented with multiple ICs which are

20   interconnected with connections which have a relatively large bandwidth.

        Fig. 1B schematically shows an embodiment of the image processor 101 comprising a switch 130 with:

                    - a first input connector that is coupled to the motion estimator 104 via motion vector path 114;

25   - a second input connector that is coupled to the external unit 108 via motion vector path 120; and

                    - an output connector that is coupled to the motion compensation unit 106, and the switch (130) having:

                    - a first state in which the first input connector is connected to the output

30   connector, enabling the further motion vector field to be provided directly from the motion estimator 104 to the motion compensation unit 106; and

                    - a second state in which the second input connector is connected to the output connector enabling the further motion vector field to be provided from the external unit 108 to the motion compensation unit 106.

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The motion estimator 104 comprises a first control interface 134 in order to enable and/or disable the motion estimator 104 and the motion compensation unit 106 comprises a second control interface 132 in order to enable and/or disable the motion compensation unit 106. A main part of the timing and control of the motion estimator 104 and of the motion compensation unit 106 is executed externally to these units 104,106.

The memory unit 102 comprises a first sub-unit 103 for storing the first input image and a second sub-unit 105 for storing the second input image.

The image processor 101 is arranged to exchange the motion vector field from the motion estimator 104 to the external unit 108 via the motion vector paths 113 respectively 124.

In connection with Fig. 2, Fig. 3A and Fig. 3B it will be described under which conditions the switch is in the first or the second state and whether the motion estimator 104 and motion compensation unit 106 are enabled or disabled.
This is summarized in Table 1.

Table 1:

	One pass (see Fig. 2)	First pass of two passes (see Fig. 3A)	Second pass of two passes (see Fig. 3B)
motion estimator 104	Enabled	Enabled	Disabled
motion compensation unit 106	Enabled	Disabled	Enabled
Switch 130	First state	Second state	Second state

Fig. 2 schematically shows the data flow 202 of the motion vector field in an embodiment of the image processor 101 running in the one pass mode. Both the motion estimator 104 and the motion compensation unit 106 are enabled as indicated with check marks 204 and 206. The switch 130 is in the first state. The sequence of processing steps is as follows. The first input image and the second input image are received from the external memory device 110 and cached in the memory unit 102 of the image processor 101. The first image, i.e. the so-called previous image, is put in sub-unit 103 and the second input image, i.e. the so-called previous image is put in sub-unit 105. The images are divided in multiple segments. For each of the segments a motion vector is calculated. All vectors of one image together form a motion vector field. These motion vectors are directly provided to the motion compensation unit 106, which calculates the motion compensated output image. In principle, the motion vectors are provided one by one or in small sets. But eventually the complete

motion vector field is provided. The advantage of providing the motion vectors one by one is
that the motion compensation unit 106 can complete the output image relatively short after
the last motion vector has been calculated. Another advantage is that no memory space is
required in the image processor 101 to store the complete motion vector field. Typically the
5   motion vectors are also stored in the external memory device 110.

Fig. 3A schematically shows the data flow 302 of the motion vector field in an
embodiment of the image processor 101 during the first pass of the two pass mode. The
motion estimator 104 is enabled and the motion compensation unit 106 is disabled as
indicated with reference numerals 304 and 306. The switch 130 is in the second state.
10   However the state of the switch 130 is not relevant because the motion compensation unit
106 is disabled. The sequence of processing steps is as follows. The first input image and the
second input image are received from the external memory device 110 and cached in the
memory unit 102 of the image processor 101. The images are divided in multiple segments.
For each of the segments a motion vector is calculated. These motion vectors are temporarily
15   stored in the external memory device 110. The external unit 108 can access these motion
vectors. The external unit 108 is designed to calculate a further motion vector field,
optionally based on the motion vectors being calculated by the motion estimator 104. The
further motion vector field calculated by the external unit 108 will be used by the image
processor 101 in the second pass. Optionally this further motion vector field is also stored in
20   the external memory device 110.

Fig. 3B schematically shows the data flow 312 of the further motion vector
field in an embodiment of the image processor 101 during the second pass of the two pass
mode. The motion estimator 104 is disabled and the motion compensation unit 106 is enabled
as indicated with reference numerals 308 and 310. The switch 130 is in the second state. The
25   sequence of processing steps is as follows. The first input image and the second input image
are received from the external memory device 110 and cached in the memory unit 102 of the
image processor 101. The particular motion vectors corresponding to the first and second
input image are provided by the external source 108 or retrieved from the external memory
110. The motion compensation unit 106 calculates the output image. The scanning direction,
30   i.e. the sequence of segments being processed, during the second pass is independent of the
scanning direction during the first pass. In other words, during the first pass motion vectors
can be calculated for segments from bottom-right to top-left of the image while during the
second pass the motion compensated output image can be created by processing segments
from e.g. top-left to bottom-right. This allows alternating the scanning directions of the

motion estimator, which increases the convergenge speed of the algorithms, while the motion compensation always applies the same scanning direction.

The external unit 108 and the image processor 101 are both designed to calculate motion vectors that are related to the same sequence of images. The image processor 101 is designed to calculate a first motion vector field of a particular image pair during a first time slot. The external unit 108 is arranged to calculate a second motion vector field of the particular image pair during a second time slot based on the first motion vector field. In a third time slot the second motion vector field will be used by the motion compensation unit 106 of the image processor 101 to calculate an output image. However the external unit 108 and the image processor 101 are processors which run in parallel. The effect of the parallel processing is illustrated with an example.

The example is summarized in Table 2.

Table 2:

Time slot	external unit 108	Image processor 101	
		motion estimator 104	motion compensation unit 106
1	$F_2(N-1,N)$	$F_1(N,N+1)$	-
2	$F_2(N,N+1)$	-	$F_2(N-1,N)$
3		$F_1(N+1,N+2)$	-
4	$F_2(N+1,N+2)$	-	$F_2(N,N+1)$
5		$F_1(N+2,N+3)$	-
6	$F_2(N+2,N+3)$	-	$F_2(N+1,N+2)$

During timeslot 1 the motion estimator 104 of the image processor 101 is calculating a motion vector field $F_1(N,N+1)$ of image pair N,N+1 while the external unit 108 is calculating a motion vector field $F_2(N-1,N)$ of image pair N-1,N. During timeslot 2 the motion compensation unit 106 of the image processor 101 is using the motion vector field $F_2(N-1,N)$ of image pair N-1,N while the external unit 108 is calculating a motion vector field $F_2(N,N+1)$ for image pair N,N+1. Notice that in this example the external unit 108 can spend more time on calculating a motion vector field than the image processor can spend. Taking also into account that in most cases only a portion of the motion vector field requires an improvement then it is convincing that the two pass mode results in improved image quality.

Fig. 4 schematically shows an image display apparatus 400 according to the invention comprising:

- a receiver 402 for receiving a sequence of images. The images may be broadcasted and received via an antenna or cable but may also come from a storage device

5   like a VCR (Video Cassette Recorder) or DVD (Digital Versatile Disk). The sequence of images is provided at the input connector 406 of the image display apparatus 400. Image sequences come in various image rates: film material in 24, 25 and 30 Hz and video usually in 50 Hz and 60 Hz;

- an image processor 101 implemented as described in connection with Fig.

10 1B; and

- a display device 404 for displaying images. The type of the display device 404 may be e.g. a CRT, LCD or PDP. The display device 404 can operate with image rates of 50, 60 or 100 Hz and can have either progressive or interlaced scanning.

It should be noted that the above-mentioned embodiments illustrate rather than

15 limit the invention and that those skilled in the art will be able to design alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be constructed as limiting the claim. The word 'comprising' does not exclude the presence of elements or steps not listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a

20 plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements and by means of a suitable programmed computer. In the unit claims enumerating several means, several of these means can be embodied by one and the same item of hardware.

CLAIMS:

1.   An image processor (100,101) for motion compensated image processing,
comprising:
           - a memory unit (102) for storing a first input image and a second input image;
           - a motion estimator (104) for estimating a motion vector field based on the
first input image and the second input image; and
           - a motion compensation unit (106) for calculating an output image based on a
further motion vector field and based on the first input image and the second input image,
characterized in being designed to selectively receive the further motion vector field from:
           - the motion estimator (104); or from
           - an external unit (108).

2.   An image processor (100,101) as claimed in Claim 1, characterized in that the
image processor (100,101) is designed to provide the motion vector field to the external unit
(108) which is arranged to calculate the further motion vector field on the basis of the motion
vector field.

3.   An image processor (100,101) as claimed in Claim 2, characterized in that the
external unit (108) is arranged to recalculate a particular motion vector of the motion vector
field.

4.   An image processor (100,101) as claimed in Claim 2, characterized in
comprising a switch (130) with:
           - a first input connector that is coupled to the motion estimator (104);
           - a second input connector that is coupled to the external unit (108); and
           - an output connector that is coupled to the motion compensation unit (106),
the switch (130) having:
           - a first state in which the first input connector is connected to the output
connector; and

- a second state in which the second input connector is connected to the output connector.

5. An image processor (100,101) as claimed in Claim 2, characterized in that the motion estimator (104) comprises a first control interface (134) in order to enable and/or disable the motion estimator (104).

6. An image processor (100,101) as claimed in Claim 2, characterized in that the motion compensation unit (106) comprises a second control interface (132) in order to enable and/or disable the motion compensation unit (106).

7. An image processor (100,101) as claimed in Claim 1, characterized in that the motion compensation unit (106) is designed to perform at least one of the following operations:

- de-interlacing;
- temporal image interpolation; or
- temporal noise reduction.

8. An image display apparatus (400) comprising:
- a receiver (402) for receiving a sequence of images comprising a first input image and a second output image;
- an image processor (100,101) for motion compensated image processing, comprising:
* a memory unit (102) for storing the first input image and the second input image;
* a motion estimator (104) for estimating a motion vector field based on the first input image and the second input image; and
* a motion compensation unit (106) for calculating an output image based on a further motion vector field and based on the first input image and the second input image;
- a display device (404) for displaying the output image, characterized in that the image processor (100,101) is designed to selectively receive the further motion vector field from:
- the motion estimator (104); or from
- an external unit (108).

9.   An image display apparatus (400) as claimed in Claim 8, characterized in that that the image processor (100,101) is designed to provide the motion vector field to the external unit (108) which is arranged to calculate the further motion vector field on the basis of the motion vector field.

10.   An image display apparatus (400) as claimed in Claim 8, characterized in that the motion compensation unit (106) is designed to perform at least one of the following operations:
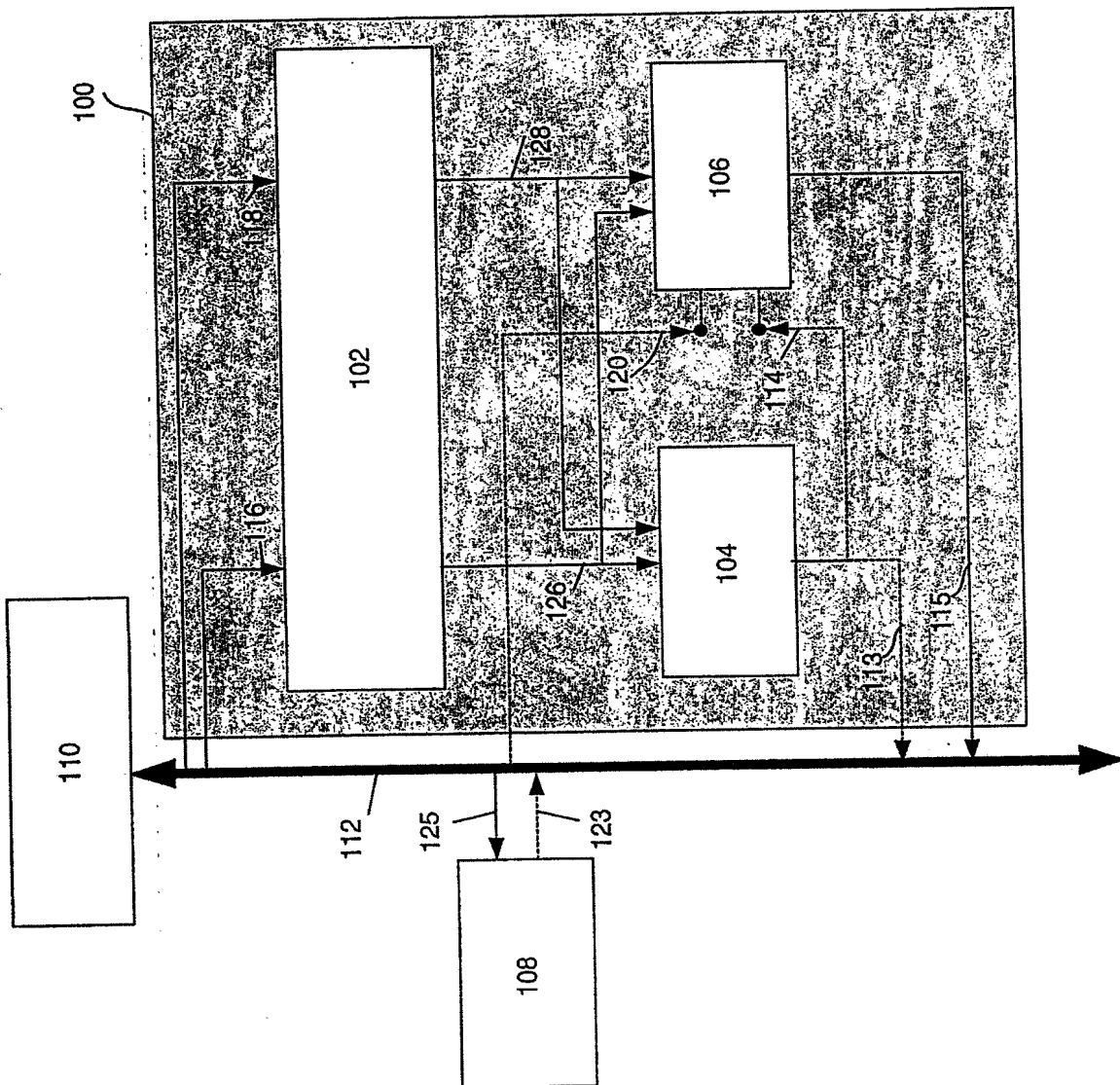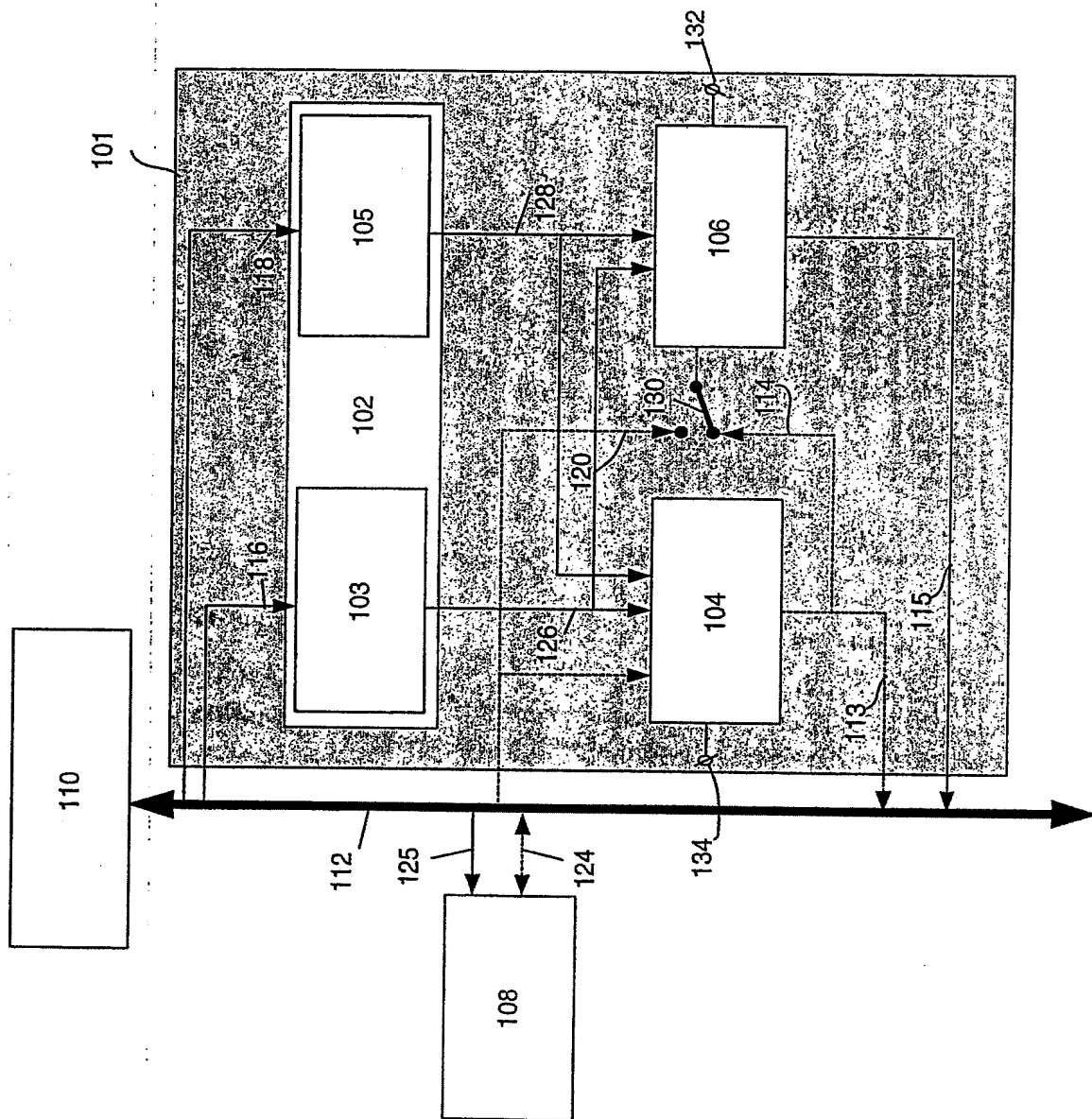
- de-interlacing;
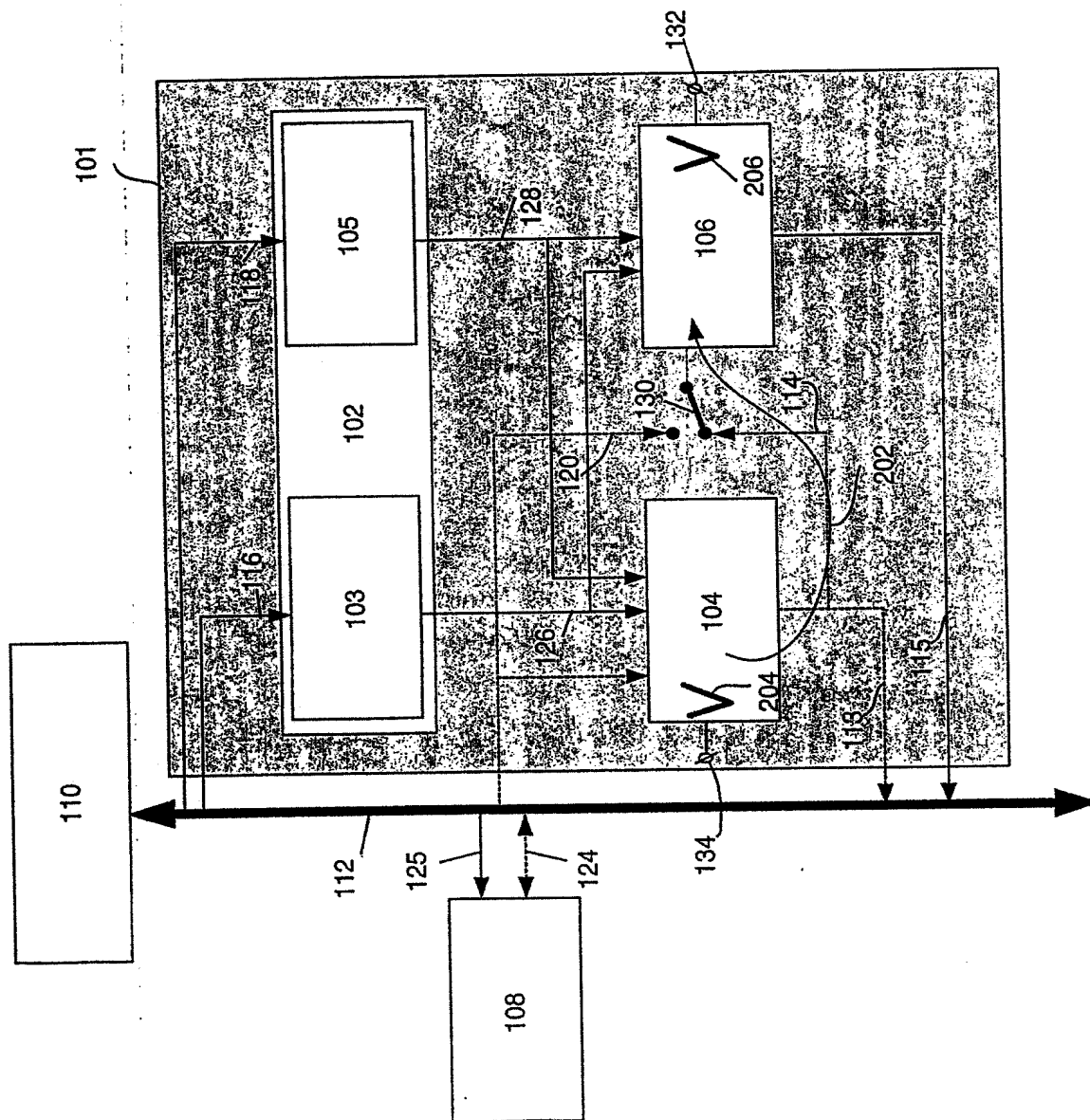- temporal image interpolation; or
- temporal noise reduction.
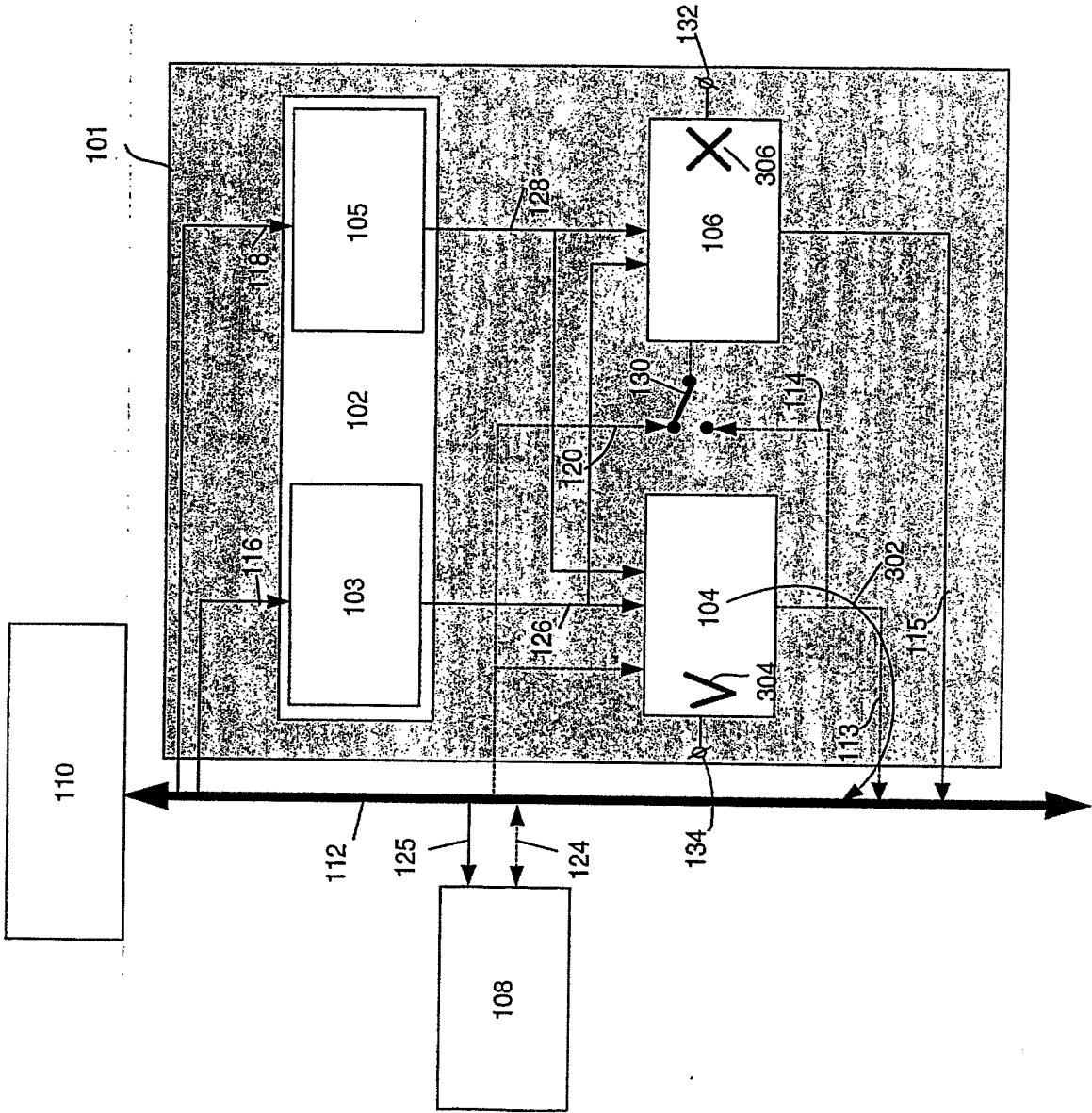
FIG.1A

FIG.1B

FIG.2

FIG.3A
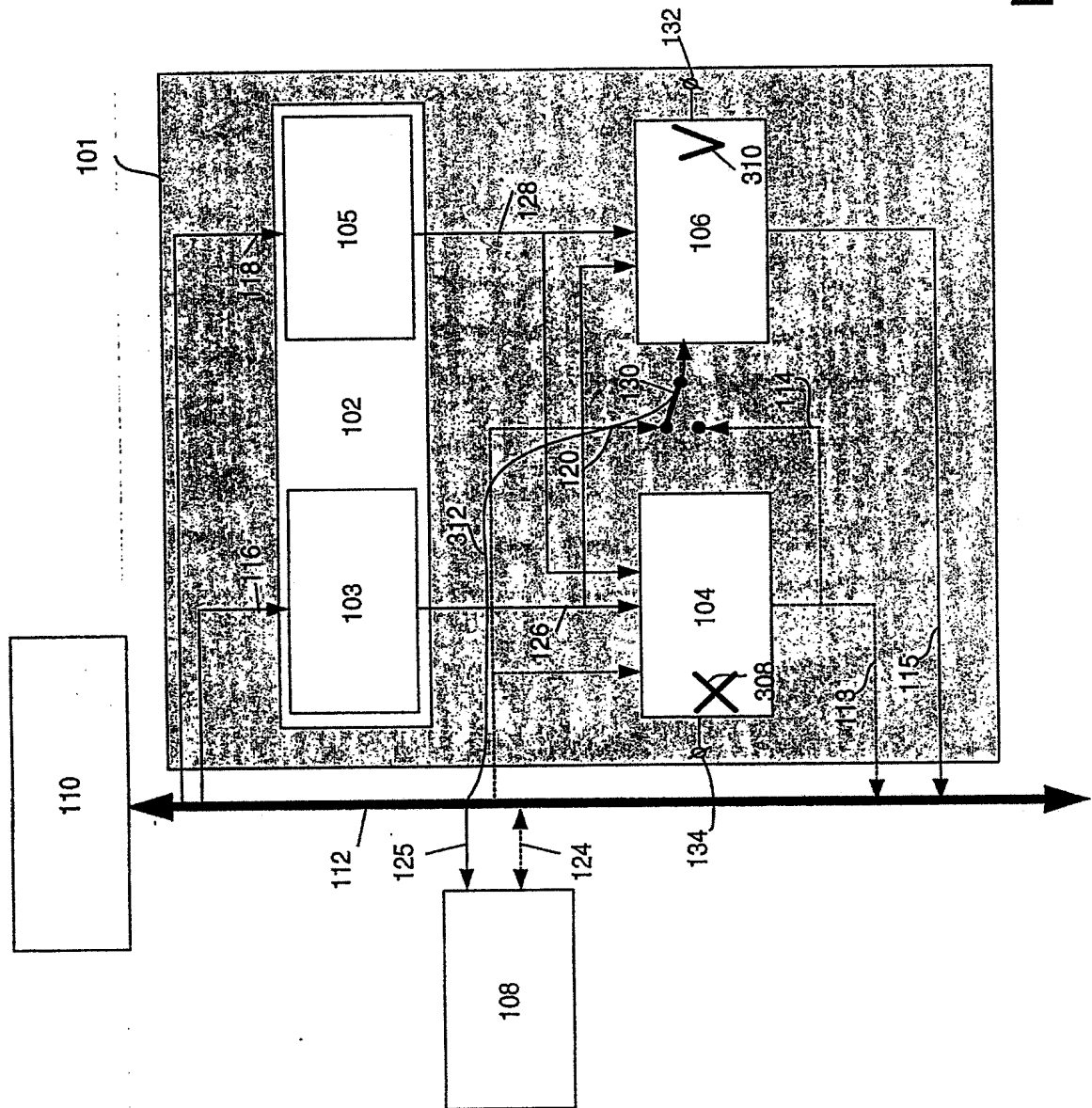
FIG.3B
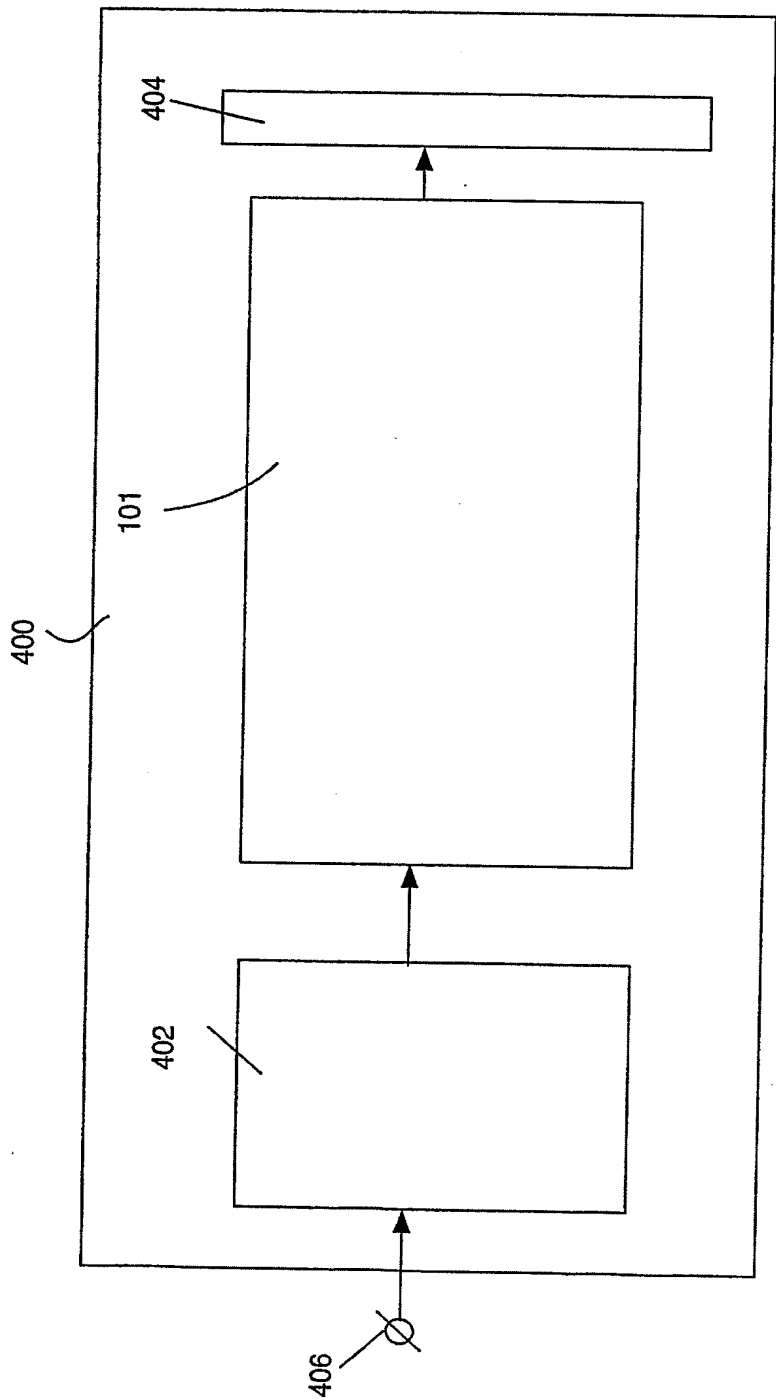
FIG. 4

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7   H04N7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7   H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 091 460 A (MISHIMA HIDETOSHI ET AL) 18 July 2000 (2000-07-18) column 6, line 5 -column 7, line 41; figure 8	1-10
A	US 6 147 718 A (TAKASHIMA MASATOSHI ET AL) 14 November 2000 (2000-11-14) column 8, line 27 -column 9, line 42; figure 1	1-10
A	US 5 687 097 A (MIZUSAWA HIDEYUKI ET AL) 11 November 1997 (1997-11-11) column 4, line 30 -column 5, line 6; figure 2	1-10

☐	Further documents are listed in the continuation of box C.	X	Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not
    considered to be of particular relevance
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    filing date
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    which is cited to establish the publication date of another
    citation or other special reason (as specified)
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    other means
"P" document published prior to the international filing date but
    later than the priority date claimed

"T" later document published after the international filing date
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    cited to understand the principle or theory underlying the
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"X" document of particular relevance; the claimed invention
    cannot be considered novel or cannot be considered to
    involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention
    cannot be considered to involve an inventive step when the
    document is combined with one or more other such docu-
    ments, such combination being obvious to a person skilled
    in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2002	14/11/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Luckett, P

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